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A simple digital readout circuit for differential resistive or capacitive sensors

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Abstract

This paper introduces and analyzes a novel direct interface circuit (DIC) that directly connects differential resistive and capacitive sensors to digital processors (DPs), performing a magnitude-to-time-to-digital conversion of the information they provide. The simple circuit performs the readout using two passive components, the differential sensor and the DP. In some cases, the circuit may require an additional passive element. The DP only uses common digital resources such as bidirectional pins or a counter, meaning microcontrollers, FPGAs, or ASICs could all be used as DPs. Different DICs proposed in the literature for reading differential sensors require three time measurement processes to estimate the variable to be measured. The new circuit requires only one, saving time and energy dissipation and reducing the number of error sources. A design based on an FPGA has been implemented as a proof of concept. Measurement times in the order of 1.1–1.3 ms have been obtained with this configuration. Errors in the readout of a differential resistive sensor are below 0.34% in the worst case and below 0.63% for a differential capacitive sensor.

(Some figures may appear in colour only in the online journal)

1. Introduction

Sensors are now ubiquitous, especially since the explosion of the Internet of Things (IoT) or Ambient Intelligence applications (AmI). As the number of sensors used in these applications increases, there is a growing demand for readout circuits that consider their requirements. The ideal solution would be that these circuits were simple (reducing their size and cost), with low power consumption (so the sensors can be included in portable devices with small batteries), and with short measurement times (to meet increasing demands for speed). Moreover, IoT or AmI circuits use a digital processor (DP) as their core (either a microprocessor, an FPGA, or an ASIC) to coordinate and control information receiving, sending, and processing. Therefore, it is interesting that the DP directly acquires the sensor's information.

Some interesting types of sensors are called differential resistive or capacitive sensors (DRS or DCS). These sensors are internally formed, in turn, by two sensor elements, in which the physical magnitude to be measured is transformed into an electrical magnitude (resistance or capacitance). The operation of differential sensors is based on the fact that a variation of the physical magnitude to be measured is transformed into a variation with the same sign in an electrical magnitude in one of the two sensing elements. In contrast, in the other, a variation of the opposite sign occurs for the same electrical

magnitude. Due to their construction, the DRS and DCS have three terminals, of which only one provides the information of the magnitude to be measured.

Other types of differential sensors provide a differential output. In this case, the information of the magnitude to be measured is given by the difference between the two output signals. These sensors typically have a Wheatstone bridge configuration with a variable number of sensing elements [1–5]. These devices have four terminals, two of which are used to connect the power supply.

This work focuses on the first type of sensor with three terminals. They are used, in the case of DCS, for measuring linear displacement and pressure differences [6], and for determining angular position [7, 8] and acceleration [9, 10]. DRSs are used in applications such as environmental monitoring [11], speed measurement [12], to sense linear or angular position displacement [13], and in rehabilitation devices [14]. These sensors also have inherent benefits, such as canceling the effects of temperature changes. It is, therefore, increasingly common for differential sensors to appear in IoT or AmI. This situation means that specific readout circuits for these sensors must be designed to comply with the characteristics set out above.

Figure 1 shows the equivalent DRS and DCS circuits. The variables x_R and x_C in the figure show information about the magnitude of the physical phenomenon to be measured (x_R in the case of DRS, and x_C for DCS; x_R and $x_C \in (-1,1)$). As shown in figure 1, two possibilities relate x_R and x_C to the electrical circuit. In the case of the linear relationship, the elements of the differential sensor are given by

$$R_m = \frac{R_S}{2}(1 - x_R), \quad R_M = \frac{R_S}{2}(1 + x_R) \qquad (1)$$

$$C_m = \frac{C_S}{2}(1 - x_C), \quad C_M = \frac{C_S}{2}(1 + x_C) \qquad (2)$$

where R_S and C_S are characteristic constant parameters of each DRS or DCS, respectively.

If the relationship is hyperbolic, we have

$$R_m = \frac{R_S}{2(1 + x_R)}, \quad R_M = \frac{R_S}{2(1 - x_R)} \qquad (3)$$

$$C_m = \frac{C_S}{2(1 + x_C)}, \quad C_M = \frac{C_S}{2(1 - x_C)}. \qquad (4)$$

There are also sensors with two internal elements in which the electrical magnitude of one of them varies in the same way as the physical magnitude to be measured (increasing or decreasing with it). In contrast, the electrical magnitude remains constant in the other, being taken as a reference value [15]. Although these sensors cannot exactly be considered differential sensors, they can be used as those with a hyperbolic relationship.

To obtain x_R, the seminal work by Owen [16] proposes using an integrator circuit built with an operational amplifier (OA), two voltage sources, four switches, and an analog comparator. Most recent proposals also use various OAs, analog
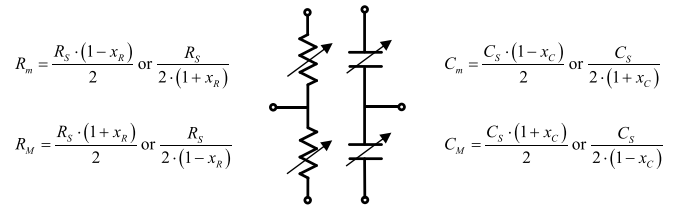

Figure 1. Equivalent circuit for differential resistive and capacitive sensors.

comparators, switches, and passive elements [17–22]. Errors in these proposals range from 0.35%–1.18% full-scale span (FSS), while the measurement times, T_M, are between 30 ms and 100 ms (in the references that provide the datum).

In the case of DCS, most proposals use different versions of a relaxation-oscillator and AC sources to find x_C [23–27]. Errors are between 0.1% and 6.74% FSS. Only [23] reports a T_M of 4.4 ms.

Except for [21, 22], all proposed DRS or DCS readout circuits need to include an analog-to-digital converter (ADC) to provide the information to the DP. On the other hand [21, 22], require a digital complex filter in addition to OAs and comparators.

Direct interface circuits (DICs) were introduced in [30, 31] to reduce the complexity of the readout circuits of different types of sensors. DICs do not require an intermediate signal conditioner (based on amplifiers or oscillators) or an ADC, but rather just some passive elements to connect the sensor directly to a DP. All DICs perform a magnitude-to-time-to-digital conversion. This type of design is employed in [28] for DRS readout, figure 2(a). The circuit performs three charges and discharges of C and three time measurements to determine x_R. All pins in figure 2(a) are configured as output pins with a logical 1 output during charging. We call V_{ch} the maximum voltage a DP pin can reach, which, in this case, will match the maximum voltage stored in the capacitor. A discharge follows each charge. During discharging, only one pin P_o, P_m, or P_M is with a logical 0 output. The other pins are configured as high impedance state inputs, HZ. The time interval from the discharge start until node V_C in figure 2(a) reaches voltage V_{TL} is measured for each discharge. V_{TL} is the threshold voltage to detect a logical 0 input in pin P_1 starting from a logical 1 level. The length of the discharge steps is measured in DP clock cycles with period T_{CK}, obtaining three values: T_o, T_m, and T_M (the subscript indicates the pin with a logical 0 output level). Each of these times has the form

$$T_i = (R_i + \text{ro})\, C \ln\left(\frac{V_{ch}}{V_{TL}}\right) \qquad (5)$$

where R_i is the equivalent resistor through which the discharge is made, and ro is the output resistance of each pin configured as a logic 0 output. Considering (5) and the expressions (1) or (3), it is easy to find

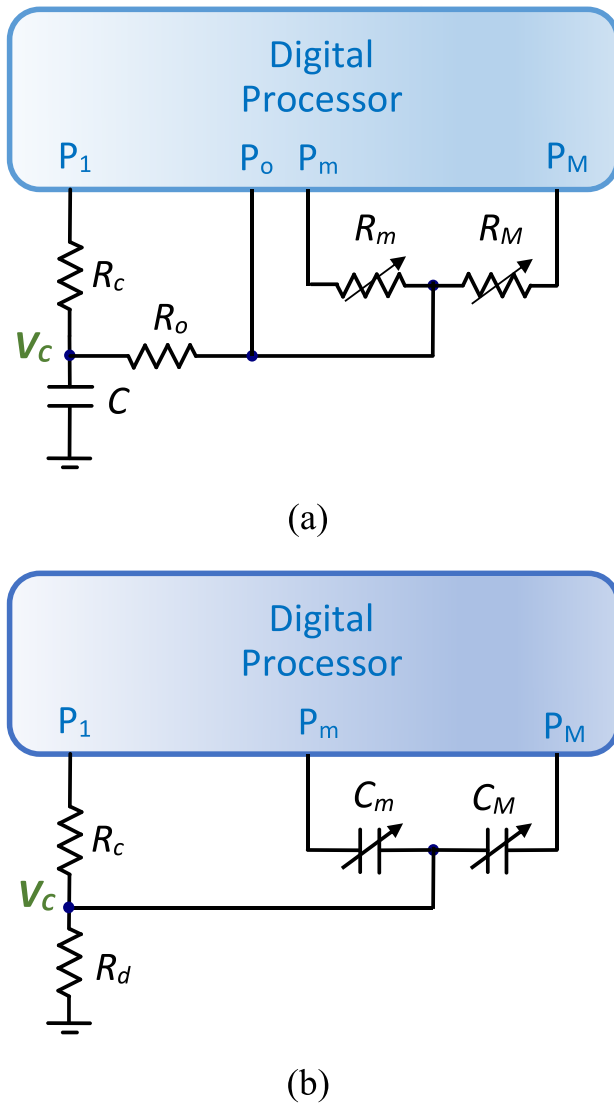$$x_R = \frac{T_M - T_m}{T_M + T_m - 2T_o}. \qquad (6)$$

(a)

(b)

Figure 2. Scheme of the DICs proposed in the literature (a) for the readout of differential resistive sensors [28] (b) for the readout of differential capacitive sensors [29].

This method to obtain x_R is simple but has some drawbacks. Three capacitor charges are required (each charge consumes energy and time). Moreover, the charges must last long enough to ensure V_{ch} is identical at the start of the three discharges (R_c is introduced primarily to improve equality between these final charge voltages [32]). Furthermore, (6) assumes that ro is the same for pins P_o, P_m, and P_M when there may be differences between them. In [28], the authors provide x_R errors of 0.42% FSS obtained after an offline calibration with $T_M = 1.84$ ms.

A DIC for the DCS readout is shown in figure 2(b) [29]. Again, the circuit performs three charging and discharging steps to determine x_C. However, a different capacitor is used in each charging and discharging step. Discharges always occur through resistor R_d (this resistance does not need to be precisely known, although $R_d \gg R_C$ is essential for proper circuit operation). In this circuit, the discharge times T_m, T_M, and

T_{m+M} (where the subscript indicates the capacitor being discharged) take the form

$$T_i = R_d C_i \ln \left(\frac{V_{ch}}{V_{TL}} \right). \tag{7}$$

where C_i is the equivalent capacitor through which discharge is carried out. From (7) and (2) or (4) we have

$$x_C = \frac{T_M - T_m}{T_{m+M}}. \tag{8}$$

The method to find x_C using (8) is also simple. Still, it has the same drawbacks as discussed above for [28], reporting a maximum error of 1.1% FSS (after an offline calibration) for a single-axis accelerometer and an overall T_M of around 50 ms.

This paper presents a new type of DIC that requires a single charge and discharge process to estimate x_R or x_C. The basic idea is to take the three necessary time measurements to get the estimates during the single discharge process (this idea was already introduced in [33] with two time measurements for a simple capacitive sensor). This procedure will reduce measurement time, power consumption, and sources of error, such as the possible differences in V_{ch} between charging processes or the different values of ro in the different pins. Under certain conditions, the new proposal also has the advantage of the circuit topology being the same for the DRS and the DCS readouts, meaning a single implementation could interchange the sensors to be read. As the new DIC needs only a few passive components, which improve the cost and reliability of the circuit, the circuit is an exciting candidate for IoT and AmI.

2. New differential sensor readout circuit

The new read circuits for DRS or DCS are shown in figure 3. The circuit has a resistive branch with two resistors in series and a capacitive branch with two capacitors in series. Therefore, these branches have equivalent impedances, $R_T = R_A + R_B$ and $C_T = C_A \parallel C_B$. For DRS readout, the sensor forms the resistive branch, and known discrete capacitors form the capacitive branch. For DCS readout, the sensor comprises the capacitive branch, and known discrete resistors form the resistive branch. Circuit operation for reading the two types of sensors is described below.

2.1. Differential resistive sensor readout

For DRS readout, resistor R_A in figure 3 will be one of the sensor resistors, let us assume R_m, while R_B will be R_M. The designer chooses C_A and C_B with known capacitances (selection rules for these capacitors will be established later). The steps necessary to perform the DRS readout and the waveforms of voltages V_J, V_C, and V_R in figure 3 are shown in figure 4.

In step 1 in figure 4, both capacitors are entirely discharged for time T_{dis} to ensure $V_J = V_C = 0$. In step 2, charging is performed for time T_{ch}, setting P_J as logical 1 output and P_C
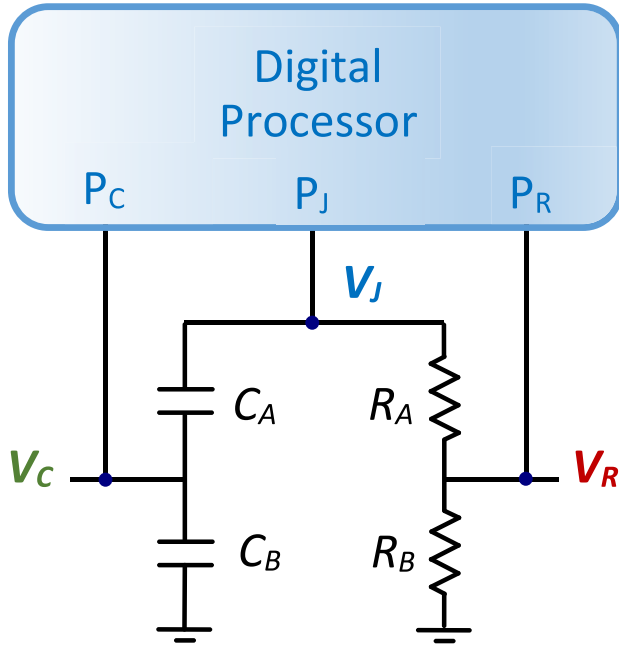
Figure 3. Proposed DIC for the readout of differential resistive or differential capacitive sensors.
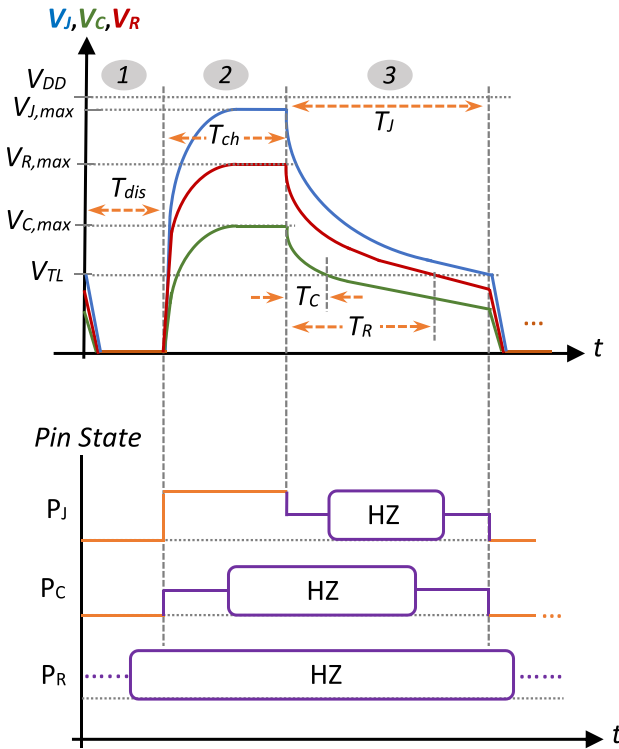

Figure 4. Waveforms and pin states for the circuit of figure 3.

and P_R pins in HZ state. At the end of step 2, $V_J = V_{J,\max}$, this being close to V_{ch} but slightly lower due to the presence of the resistive branch. The maximum voltages for V_C and V_R ($V_{C,\max}$ and $V_{R,\max}$) are given by

$$V_{C,\max} = V_{J,\max} \cdot \frac{C_A}{C_A + C_B} \tag{9}$$

$$V_{R,\max} = V_{J,\max} \cdot \frac{R_M}{R_m + R_M}. \tag{10}$$

For correct circuit operation, it makes no difference which of the two voltages is higher (this will depend on x_R and the values selected for C_A and C_B). The only important thing is that both values are greater than V_{TL}, so they are detected as a logical 1 when starting the discharging process (step 3 in figure 4). During discharge, the voltages in the different nodes are given by [34]

$$V_i = V_{i,\max} \cdot e^{\frac{-t}{R_T \cdot C_T}}; \quad i \in \{J, C, R\}. \tag{11}$$

With these equations, we find the instants at which V_J, V_C, and V_R voltages reach the value V_{TL}. If we call these instants T_J, T_C, and T_R, respectively (as in figure 4), we find

$$T_J = R_T \cdot C_T \cdot \ln\left(\frac{V_{J,\max}}{V_{TL}}\right) \tag{12}$$

$$T_C = R_T \cdot C_T \cdot \ln\left(\frac{C_A}{C_A + C_B} \frac{V_{J,\max}}{V_{TL}}\right) \tag{13}$$

$$T_R = R_T \cdot C_T \cdot \ln\left(\frac{R_M}{R_m + R_M} \frac{V_{J,\max}}{V_{TL}}\right) \tag{14}$$

resulting

$$\frac{T_R - T_J}{T_J - T_C} = \frac{\ln\left(R_M/(R_m + R_M)\right)}{\ln\left(1 + C_B/C_A\right)}. \tag{15}$$

The denominator on the right-hand side of (15) is known and will be denoted as k_C. With this, we can rewrite (15)

$$x_R = 2e^{k_C \frac{T_R - T_J}{T_J - T_C}} - 1. \tag{16}$$

This is the estimating equation of x_R, valid for both linearly and hyperbolically related DRS.

2.2. Differential capacitive sensor readout

For DCS readouts, the designer chooses the values for R_A and R_B, the selection criteria presented later. C_A plays the role of the capacitor C_m and C_B the role of C_M. The readout process is still as shown in figure 4. Hence, T_J is also obtained from (12) (with the new values of R_T and C_T), while T_C, and T_R are

$$T_C = R_T \cdot C_T \cdot \ln\left(\frac{V_{J,\max}}{V_{TL}} \cdot \frac{C_M}{C_m + C_M}\right) \tag{17}$$

$$T_R = R_T \cdot C_T \cdot \ln\left(\frac{V_{J,\max}}{V_{TL}} \cdot \frac{R_B}{R_A + R_B}\right). \tag{18}$$

As with (15), we find

$$\frac{T_J - T_C}{T_R - T_J} = \frac{\ln\left(C_M/(C_m + C_M)\right)}{\ln\left(1 + R_A/R_B\right)}. \tag{19}$$

The denominator on the right-hand side of this equation is known and will be denoted as k_R. Thus,

$$x_C = 2e^{k_R \frac{T_J - T_C}{T_R - T_J}} - 1. \tag{20}$$

This is the estimating equation of x_C with a linear or hyperbolic relationship.

On the other hand, proper operation of the new circuit requires $V_{C,\max}$, and $V_{R,\max}$ to be greater than V_{TL}. This implies that the following must be valid for DRS

$$V_{C,\max} = V_{J,\max} \cdot \frac{C_A}{C_A + C_B} \approx V_{\text{ch}} \cdot \frac{C_A}{C_A + C_B} > V_{\text{TL}} \tag{21}$$

$$V_{R,\max} = V_{J,\max} \cdot \frac{R_M}{R_m + R_M} \approx V_{\text{ch}} \cdot \frac{(1 + x_R)}{2} > V_{\text{TL}} \tag{22}$$

or for DCS

$$V_{R,\max} = V_{J,\max} \cdot \frac{R_B}{R_A + R_B} \approx V_{\text{ch}} \cdot \frac{R_B}{R_A + R_B} > V_{\text{TL}} \tag{23}$$

$$V_{C,\max} = V_{J,\max} \cdot \frac{C_M}{C_m + C_M} \approx V_{\text{ch}} \cdot \frac{(1 + x_C)}{2} > V_{\text{TL}}. \tag{24}$$

Making the right choice of R_A and R_B, or C_A and C_B ensures (21) and (23) are met. These equations constitute the circuit design rules. However, compliance with (22) and (24) limits the range of values of x_R and x_C, since

$$x_R, x_C > 2 \cdot \frac{V_{\text{TL}}}{V_{\text{ch}}} - 1. \tag{25}$$

For most DPs, V_{TL} is less than half of V_{ch}, so x_R and x_C can take any positive value but not all negative values. The experimental results section will show x_R and $x_C \in (-0.2, 1)$ in our implementation. This is sufficient for a large number of DRSs or DCSs (e.g., x_R and x_C are included in the range -0.2 and 0.2 in [23, 24, 26, 35, 36]). However, in applications with more negative values of x_R and x_C, it is necessary to modify the circuit in figure 3.

2.3. Modifying the readout circuit for an extended range of x_R or x_C

Figure 5(a) shows the modified circuit to estimate $x_R \in (-1, 1)$, and figure 5(b) for $x_C \in (-1, 1)$. The designer chooses resistance R_E and capacitance C_E.

Assuming DRS with a linear relationship, the circuit in figure 5(a) can be used in the same way as in figure 3, considering two new resistors (framed in dashed rectangles), R'_m and R'_M, which would form a new fictitious differential sensor in which the magnitude to be measured would be given by x'_R. The following relationships are therefore verified

$$R'_m = \frac{R'_S}{2}(1 - x'_R) = R_m = \frac{R_S}{2}(1 - x_R) \tag{26}$$

$$R'_M = \frac{R'_S}{2}(1 + x'_R) = \frac{R_S}{2}(1 + x_R) + R_E \tag{27}$$
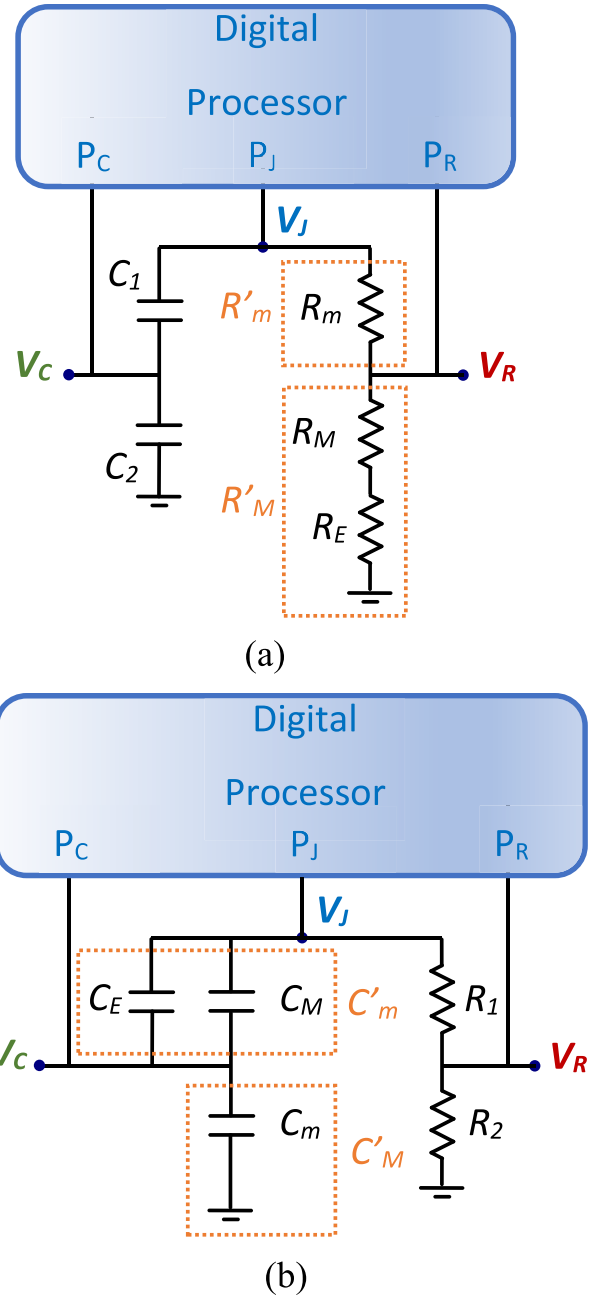

(a)

(b)

Figure 5. Modifications of the new DIC if x_R and $x_C \in (-1, 1)$ (a) for the readout of DRS, (b) for DCS.

$$R'_S = R_S + R_E. \tag{28}$$

From (26)–(28), we can find the relationship between x_R and x'_R

$$x_R = \left(1 + \frac{R_E}{R_S}\right) x'_R - \frac{R_E}{R_S}. \tag{29}$$

If measurements T_J, T_C, and T_R are performed in the circuit in figure 5(a) (whose equations are still (12), (13) and (14), respectively, but with $R_T = R_S + R_E$ and substituting R_m and

R_M with R'_m and R'_M) x'_R is still obtained from the right-hand side of (16). Then, as R_S can be known from T_J and T_C

$$T_J - T_C = (R_S + R_E) k_C (C_A \parallel C_B) \tag{30}$$

and substituting its value in (29), we obtain x_R as a function of time measurements and constants selected by the designer

$$x_R = \frac{(T_J - T_C)(1 + x'_R) - \tau_{\mathrm{RE}}}{(T_J - T_C) - \tau_{\mathrm{RE}}} \tag{31}$$

where τ_{RE} is

$$\tau_{\mathrm{RE}} = k_C R_E (C_A \parallel C_B). \tag{32}$$

Following similar steps above, it is easy to show that (31) is also valid for DRS with a hyperbolic relationship.

A minimum value of R_E, $R_{E,\min}$, ensures that $x_R = -1$ can be measured. For example, for DRS with a linear relationship, $R_{E,\min}$ can be found from the expression equivalent to (22) for the circuit in figure 5(a)

$$V_{J,\max} \cdot \frac{R'_M}{R'_m + R'_M} = V_{J,\max} \cdot \frac{R_{E,\min}}{R_S + R_{E,\min}} > V_{\mathrm{TL}} \tag{33}$$

resulting in

$$R_{E,\min} > \frac{R_S}{\frac{V_{J,\max}}{V_{\mathrm{TL}}} - 1} \approx \frac{R_S}{\frac{V_{\mathrm{ch}}}{V_{\mathrm{TL}}} - 1}. \tag{34}$$

According to this, $R_{E,\min}$ depends on the chosen DP and the sensor's total resistance.

The new circuit for DCS with x_C. $\epsilon (-1,1)$ is shown in figure 5(b) with two new equivalent capacitors, C'_M and C'_m, of a new fictitious differential sensor and a new measurement magnitude, x'_C. If the sensor is linear, an equation equivalent to (29) is verified

$$x_C = \left(1 + \frac{C_E}{C_S}\right) x'_C - \frac{C_E}{C_S}. \tag{35}$$

The following is also true

$$C_T = \frac{C'_M \cdot C'_m}{C'_M + C'_m} = \frac{(C_M + C_E)C_m}{C_S + C_E} \tag{36}$$

$$T_J - T_C = k_R (R_A + R_B) C_T. \tag{37}$$

Equations (35)–(37) give x_C

$$x_C = \frac{4(T_J - T_R) x'_C - \tau_{\mathrm{CE}} (1 - x'_C)}{4(T_J - T_R) - \tau_{\mathrm{CE}} \left(1 - x'^2_C\right)} \tag{38}$$

where x'_C is estimated by substituting measurements T_J, T_C, and T_R (taken in the circuit of figure 5(b)) on the right side of (20) and τ_{CE} is

$$\tau_{\mathrm{CE}} = k_R (R_A + R_B) C_E. \tag{39}$$

A procedure like the above provides for DCS with a hyperbolic relationship

$$x_C = 1 - \frac{4\tau_{\mathrm{CE}} (1 - x'_C)}{4\tau_{\mathrm{CE}} - \left(1 - x'^2_C\right)(T_J - T_R)}. \tag{40}$$

An equivalent equation to (34) also provides the minimum value of C_E, $C_{E,\min}$, to estimate $x_C \epsilon (-1,1)$

$$C_{E,\min} > \frac{C_S}{\frac{V_{J,\max}}{V_{\mathrm{TL}}} - 1} \approx \frac{C_S}{\frac{V_{\mathrm{ch}}}{V_{\mathrm{TL}}} - 1}. \tag{41}$$

For both DRS and DCS, the cost of extending the range of x_R and x_C while maintaining a single charging–discharging process has been the introduction of a single additional passive component.

2.4. Errors, uncertainty, and resolution

As discussed, the new proposal eliminates some sources of error in [28] and [29]. The first one is the difference between the final voltages of each charging process. These differences are unavoidable due to noise in the circuit. In [28] and [29] an attempt is made to minimize these differences by lengthening the charging times. In the new proposals, since there is only one charging process, this is not necessary, thus reducing T_M. On the other hand, ro is no longer a source of error in the new proposals since its only effect is to determine the closeness between $V_{J,\max}$ and V_{DD}.

However, the presence of stray capacitors is inevitable. By the very nature of these capacitors, the errors they introduce in the estimates of x_R or x_C are highly variable over the entire range, producing the sensation of random errors in the circuits of figures 2, 3, and 5. Beyond the careful implementation of circuit routing, little can be done to reduce these errors.

On the other hand, unlike in [28] and [29], to estimate x_C in the new circuit, it is necessary to know precisely the values of the passive resistances R_A and R_B. Similarly, the values of the passive capacitors C_A and C_B must be known precisely to estimate x_R. For this reason, these elements must be high-precision components that are as stable as possible against temperature variations and aging. Thus, the errors that can be introduced by variations in the values of these elements will be minimal.

The noise introduced by the power supply also affects the V_{TL} value of an input pin, causing it to vary. This phenomenon is known as trigger uncertainty, u_{trigger} [32], and it also affects the estimate provided by the circuits in figure 2.

In [37], it is found that, for any time measurement, u_{trigger} is inversely proportional to the value of the voltage slope in the measurement pin when this voltage reaches the value V_{TL}. From (11) it can be deduced that u_{trigger} has the same form in all time measurements

$$u_{\mathrm{trigger}}(T_i) \propto R_T C_T; \quad i \in \{J, C, R\}. \tag{42}$$

The product $R_T C_T$ is not related to x_R only when the circuits in figures 3 or 5 are used for DRS with a linear relationship.

In hyperbolic relationship, different x_R or x_C imply different values of $R_T C_T$, meaning $u_{\text{trigger}}(T_i)$ will vary with x_R or x_C. As $u(x_R)$ or $u(x_C)$ depend on these uncertainties, they will also change over the range of x_R or x_C.

In addition to u_{trigger}, quantization uncertainty, u_q, appears due to the measurement of the different times used in the estimates in clock cycles of the DP. This uncertainty can be ignored if all times are long enough. The designer should therefore choose sufficiently large values of C_A and C_B or R_A and R_B.

Increasing the resolution of the new circuits involves increasing the values of T_J—T_C, and T_R—T_J, which appear in (16), (20), (31), (38) and (40). This can be achieved by also increasing $R_T C_T$. However, these increases only make sense up to a specific value of $R_T C_T$ for which $u_{\text{trigger}} \gg u_q$, since, according to (42), any further rise in $R_T C_T$ brings an increase in uncertainty (along with an increase in T_M). R_E and C_E should therefore be chosen to meet (34) and (41), but making them as small as possible.

However, resolution can also be improved by maintaining a constant value of $R_T C_T$ and decreasing T_R and T_C. This can be achieved with values of R_A and R_B or C_A and C_B that provide initial values $V_R(0)$ and $V_C(0)$ as close as possible to V_{TL} (while maintaining a logical safety margin to detect them as logical 1 inputs).

3. Experimental results and discussion

A commercial printed circuit board (PCB) has been selected to verify the experimental performance of the proposed circuits, namely the CMOD A7 from Digilent (Pullman, Washington). As DP, the PCB incorporates an FPGA, the Xilinx Artix 7 XC7A35T. This PCB includes a USB-UART bridge, a clock source, 512 KB SRAM, and 4 MB Quad SPI Flash. These elements provide enough resources for the CMOD A7 to be used in applications for IoT and AmI. Using an FPGA allows different tasks to be carried out in parallel with the measurement of differential sensors. The voltage supply for the I/O pins of the FPGA is 3.3 V (this is the value of V_{DD}), and a 50 MHz clock is generated internally. However, both the rise and fall edges of the clock have been used to detect the trigger instant. This means that a new count is obtained every 10 ns. V_{TL} has been experimentally measured, finding a value of approximately 1.25 V.

The structure of the design programmed in the FPGA is shown in figure 6. The configuration of the pins, the 18-bit counter, and the three registers that store the time measurements depend on the Control Unit. A USB module has been introduced to communicate the results provided by the Arithmetic Unit to a laptop.

A series of 500 estimates of x_R or x_C has been made to present the results of this section. Various figures of merit have been derived from these measurements, characterizing the performance of the new circuits. The first one is the *maximum relative error* for the estimate of x_j (j is R or C), defined by
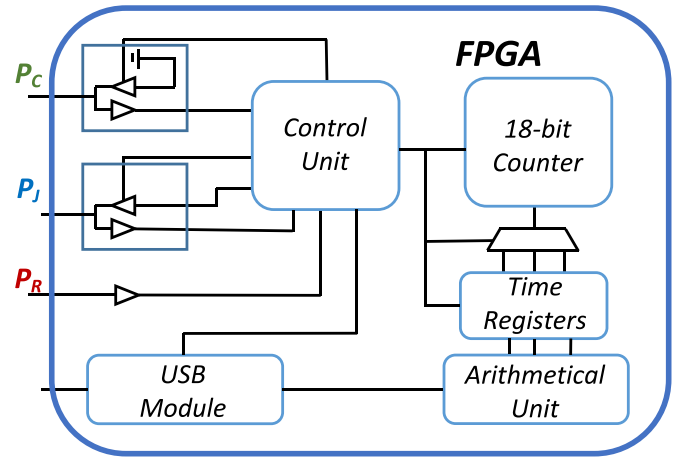

Figure 6. FPGA block diagram.

$$e_R = \text{Max}\left(\frac{|x_j(i) - x_{j,a}|}{\text{FSS}} \times 100\% \right); \quad i = \{1, 2, \ldots, 500\}. \tag{43}$$

where $x_j(i)$ is each of the estimates of x_j using (16), (20), (31) or (38), and $x_{j,a}$ is the actual value of x_j.

The second figure of merit is the *systematic error* for the estimate of x_j

$$e_S = \frac{|\overline{x_j} - x_{j,a}|}{\text{FSS}} \times 100\%. \tag{44}$$

where $\bar{x}_j$ is the average of all $x_j(i)$. Finally, the normalized uncertainty of the measurements, $u_N(x_j)$, has been obtained as a normalized standard deviation of the series of 500 measurements

$$u_N(x_j) = \frac{sd(x_j(i))}{\text{FSS}} \times 1000\%_0; i = \{1, 2, \ldots, 500\}. \tag{45}$$

To analyze the operation of the circuit in figure 3 in a more general way, it has been decided to use precision resistors and capacitors to emulate the operation of the DRS and DCS. Therefore, a combination of precision resistors has been used to obtain an approximately constant value $R_S = 12.3 \text{ k}\Omega$ with x_R varying over a range $(-0.2, 0.96)$.

The capacitors are of the CG0 type to avoid thermal drift. Selecting $C_A = 99.73$ nF and $C_B = 90.25$ nF, $V_{C,\text{max}}$ in (21) is 1.73 V > $V_{\text{TL}} = 1.25$ V (a large safety margin for the circuit to work correctly). The values of C_A and C_B were also chosen so that the results of T_R—T_J and T_J—T_C, appearing in (16), are large enough to neglect quantization errors (quantization errors less than 0.05%). As the average value of T_J was 470 μs, and 103 μs for T_C, then T_C is significantly smaller than T_J, reducing uncertainty in the estimation of x_R. $T_{\text{dis}} = 0.5$ ms was selected for the complete discharging of the capacitors, and $T_{\text{ch}} = 0.1$ ms for charging. Thus, $T_M = 1.07$ ms.

The results for $e_R(x_R)$, $e_S(x_R)$, and $u_N(x_R)$ are shown in figure 7. Note that errors e_R and e_S are shown in the left vertical
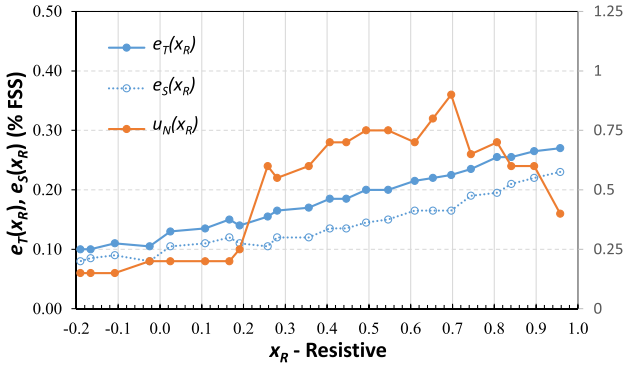
Figure 7. Relative and systematic errors, e_R and e_S (on the left Y-axis), and normalized uncertainty, u_N (on the right Y-axis), for the circuit of figure 3 when estimating $x_R \in (-0.2, 1)$.
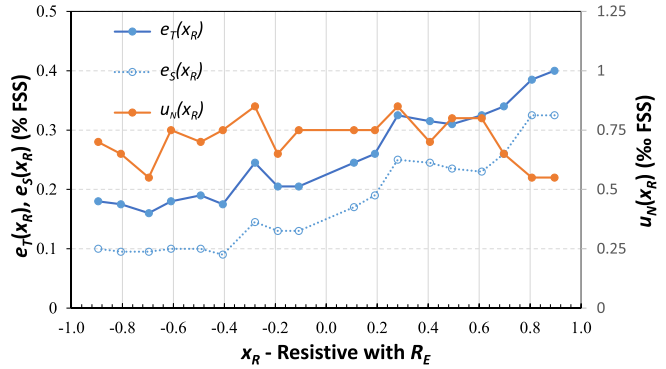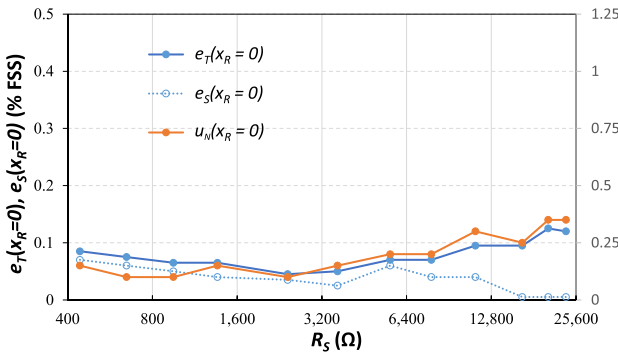

Figure 8. Values of e_R, e_S, and u_N for the circuit of figure 3 when estimating DRSs varying R_S and maintaining $x_R = 0$.

Figure 9. Values of e_R, e_S, and u_N for the new readout circuit of figure 5(a) with $x_R \in (-1, 1)$.
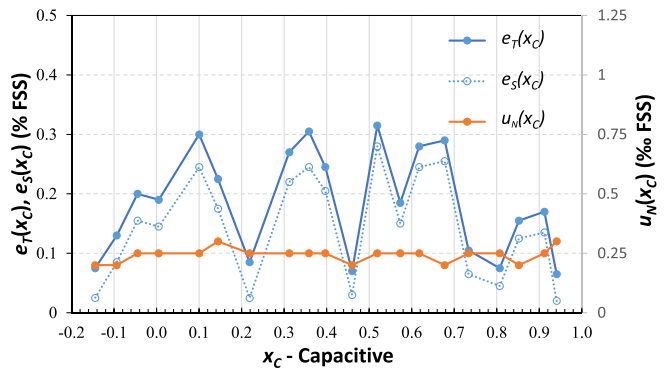

Figure 10. Values of e_R, e_S, and u_N for the new readout circuit of figure 3 when estimating DCS with $x_C \in (-0.2, 1)$.

axis for all figures with information on e_R, e_S (expressed in %, as indicated in (43) and (44)). In contrast, the right vertical axes show u_N (expressed in ‰, as indicated in (45)). The first impression when looking at figure 7 is that e_R and e_S grow as the absolute value of x_R increases. However, this growth is minimal since the maximum e_R is 0.29%, while e_S is between 0.05% and 0.24%. u_N shows little growth with x_R, varying between 0.12% and 0.21%. In any case, given the very small value of u_N relative to e_S, it has practically no effect on e_R.

It is also interesting to observe how e_R, e_S, and u_N vary when $x_R = 0$ and changes the value of R_S. The results are shown in figure 8, where 12 values of R_S ranging from 442.4 Ω to 23.584 kΩ have been taken. u_N, e_S, and e_R are practically constant in all cases.

Maintaining $R_S = 12.3$ kΩ and the values of the capacitors, $R_E = 7700$ Ω has been chosen in the circuit in figure 5(a) to allow estimation of $x_R \in (-1, 1)$. R_E is larger than the minimum of 7.5 kΩ imposed by (34), but not much larger, to avoid unnecessarily increasing u_{trigger} and, therefore, u_N. Figure 9 shows the results of these selections. In general, there is an increase with respect to figure 7 in uncertainty (due to the rise in R_T) and e_S (due to a new stray capacitor), although e_R remains below 0.34 %.

The same tests carried out for DRS have been performed for DCS. In this case, $R_A = 25\,495$ Ω and $R_B = 16\,201$ Ω

have been selected for the circuit shown in figure 3 (hence $V_{R,\text{max}} = 1.28$ V $> V_{\text{TL}} = 1.25$ V). In this case, the safety margin is only 30 mV, which is enough to ensure the circuit works correctly. The values of R_A and R_B have also been chosen so that T_J—T_C and T_R—T_J, that appear in (20), are large enough to neglect the quantization errors. Discrete CG0 capacitors have been chosen to achieve approximately $C_S = 20$ nF. With these choices, the mean value of T_J was 739 μs, while for T_R, it was 289 μs. As in the case of DRS, we have chosen $T_{\text{dis}} = 0.5$ ms and $T_{\text{ch}} = 0.1$ ms, obtaining a $T_M = 1.34$ ms.

Figure 10 shows the results. In this case, there is an erratic behavior of e_S, while u_N is practically constant. As e_S is significantly larger than u_N for many values of x_C, e_R also shows the same erratic behavior as e_S, with a maximum of 0.32%.

Figure 11 shows the results for C_S, varying between 500 pF and 34.9 nF, while $x_C = 0$. The results have peaks and troughs as in figure 10, for both e_S and u_N. Consequently, e_R again shows erratic behavior, with a high of 0.43%.

To estimate $x_C \in (-1, 1)$, maintaining $C_S = 20$ nF, of the circuit in figure 5(b), $C_E = 22.32$ nF has been used and maintained the resistance values. This value of C_E is higher than the minimum imposed by (41), 12.2 nF. Figure 12 shows the results in this case. As expected, there is an increase in uncertainty (due to the rise in C_T) and e_S (due to a new stray capacitor) compared to the values shown in figure 10. In the worst case in figure 12, e_R is 0.63%.
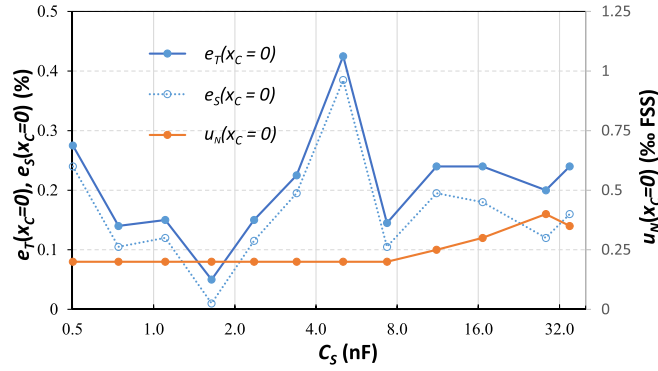
Figure 11. Values of e_R, e_S, and u_N for the new readout circuit of figure 3 when estimating DCS varying C_S and maintaining $x_C = 0$.
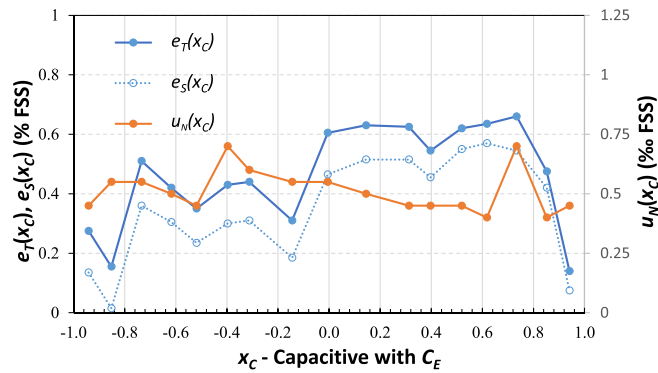

Figure 12. Values of e_R, e_S, and u_N for the readout circuit of figure 5(b) with $x_C \in (-1,1)$.

Table 1. Performance comparison.

Type	Work	x_R or x_C range	Num. pins	τ (μs)	T_M (ms)	Charge cycles	ENOB	Error (FSS%)	Voltage supply	Calibration
DRS	[28]	$(-1,1)$	4	691	1.84	3	11.3	0.42%	5 V	Offline
	This Work figure 5(a)	$(-1,1)$	3	947	1.07	1	11.4	0.34%	3.3 V	No
DCS	[29]	$(-0.07,0.07)$	3	780	50	3	7	1.1%	5 V	Offline
	This Work figure 5(b)	$(-1,1)$	3	834	1.34	1	10.8	0.63%	3.3 V	No

Finally, table 1 compares figures of merit from [28] and [29] with this work. For the DRS, the comparison considers that in [28], x_R belongs to the range $(-1,1)$ and, therefore, must be compared with the results of the circuit in figure 5(a). In [29], x_C belongs to the range $(-0.07,0.07)$. However, the comparison is made with the circuit of figure 5(b), which can estimate the full range $x_C \in (-1,1)$.

The fifth column of table 1 indicates that the largest time constants of a discharge process, τ, correspond to the new proposals, which must be considered for a fair comparison. Despite this, due to the single charge cycle, T_M is always lower on new DICs.

Table 1 shows that this work presents the best results for T_M, ENOB, and errors. It is important to note that reducing the voltage supply value implies an increase in e_R and e_S due to shorter measurement times. However, despite using the lower value of V_{DD}, the new proposals keep the errors lower. Finally, it should also be noted that the errors in [28] and [29] are calculated after an offline calibration.

4. Conclusions

A new DIC type has been proposed for reading differential resistive and capacitive sensors (DRS and DCS, respectively). Apart from the sensors, the circuit only uses a few passive components connected to a DP that performs a magnitude-to-time-to-digital conversion. The number of passive components must be increased by one, depending on the range of values of the variable measuring the physical magnitude (x_R for DRS or x_C for DCS). The DP only requires common digital resources such as bidirectional pins or a counter.

Different DICs proposed in the literature for reading differential sensors need three charge cycles to estimate x_R or x_C, while the new circuit requires only one cycle. This has important consequences as it also reduces sources of error, measurement times, and energy consumption.

A design based on an FPGA has been implemented as a proof of concept. Measurement times in the order of 1.3 ms have been obtained with this configuration. In the worst case,

the estimation errors were below 0.34% for the resistive case and below 0.63% for the capacitive case.

Thus, the new design is a simple, low-cost, fast, accurate, low-power circuit. All these features make it an ideal candidate for portable applications related to the IoT or AmI.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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